THE BASIC ATLAS PACKAGES

TECHNICAL DESCRIPTION

EP32                         APRIL 1961

# C O N T E N T S.

1.   INTRODUCTION.

Atlas is a fully-transistorised computer of package construction, a total of 3955 packages being used in the standard Atlas. With the exception of certain packages used in connection with the parallel adders, the core stores, and magnetic tape, these packages bear circuits of only seven basic types: the variations between different package types bearing the same basic circuit lie mainly in the gating provided with the circuits.

The seven basic circuits are tabulated below. The figure in brackets indicates the total number of packages based on a particular circuit actually used in Atlas.

1.   Standard inverter                                        (2128)
     (Variations: basic logical circuit           )
     (             flip-flop                       )
     (             common strobe gates             )
     (             long-tailed pair                )
     (             cable drivers and receivers)

2.   Strobe drivers                                           (89)

3.   Strobe emitter followers                                 (201)

4.   Powerful inverters
         and powerful long-tailed pairs                       (269)

5.   Decoder emitter-followers                                (287)

6.   Delays  -  short                                         (86)
                long                                          (105)

7.   Differentiators                                          (25)

These basic circuits and their variations will now be described.

2.    THE STANDARD INVERTER AND ITS VARIATIONS.

### 2.1    The basic circuit

The basic circuit of the standard inverter is shown in Fig. 1
(a complete circuit may be found on, for example, Drg. 65/52815).  The
circuit consists essentially of an OC170 transistor amplifier,
preceded by a diode gate which is of different degrees of complexity on
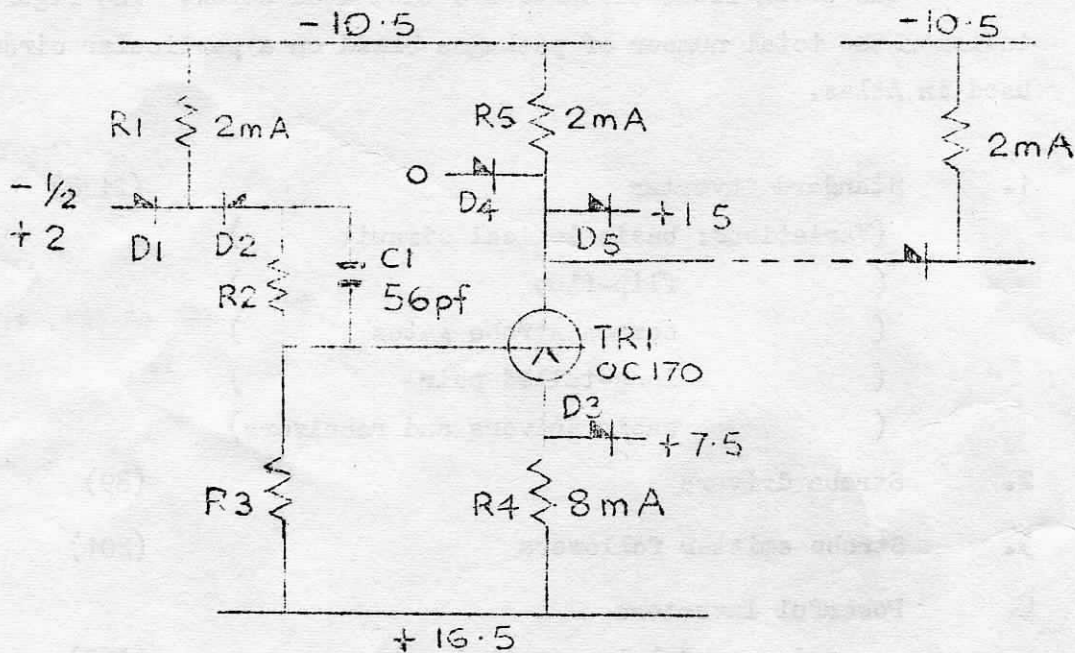different package types.



Fig. 1.

The input signal has standard levels of approximately - 1/2 v.
and + 2v.  The voltage drop caused by the AND-gate diode D1 is backed off
by the equal and opposite voltage drop caused by OR-gate diode D2, so
that these signal levels are preserved at the top of the input potentio-
meter chain, R2 and R3.  The emitter of TR1 is caught at about 8 volts
by D3 and the +7.5 v. supply, and the value of the emitter resistor is
such that a current of about 8 mA. is defined in it.

2.

The values of R2 and R3 are arranged to provide a base potential about 0.5 volts positive with respect to the emitter when the transistor is cut off by a standard positive input. In this condition the output voltage is tied to about $-1/2v$ by D4.

With a negative input level, the base voltage moves negative with respect to the potential at which the emitter is caught, and the transistor conducts. The 8 mA. previously defined in the emitter resistor is switched through the transistor, whose collector potential moves positively until it is caught at about $+2v$ by D5. The base potential now depends on the values of the input potentiometer and on the $I_b$ required to provide 8 mA. collector current. With an average value of , the base is about 0.7 v. negative with respect to the potential at which the emitter was previously caught. The total excursion of the base is thus about 1.2 volts; since the transistor requires only about 100 mV. to switch 8 mA., this represents an adequate safety factor.

The total charge which must be supplied to switch the transistor on is about 44 micro-micro-coulombs. This is made up as follows:

| | |
|---|---|
| Charge required by diffusion capacitance | 16 $\mu\mu$c |
| ($I/2\pi f_o$; for OC170 $f_o$ is about 70 Mc/s) | |
| Charge required by effective Miller capacitance | 10 $\mu\mu$c |
| ($C_{b-c} \times (\Delta V_b + \Delta V_c)$; $C_{b-c}$ is about 3 pf.) | |
| Charge required by $C_{b-e}$ when switching on | 8 $\mu\mu$c |
| (the so-called depletion capacitance effect) | |
| Charge required by stray capacitance | 10 $\mu\mu$c |
| | 44 $\mu\mu$c |

The value of C1, 56 pf., is more than adequate since with a voltage swing across it of about 1.3 v. it supplies a charge of 70 $\mu\mu$c.

The collector rise time in the absence of output wiring is about 11-13 mµS. With an output loading of about 50 pf., then with an output voltage excursion of about 2.5 volts, a charge of 125 µµs must be provided. The collector resistor is chosen to define in it a current of about 2 mA; the inverter normally feeds one or two AND-gates each with a 2 mA. load; there is thus about 4 mA. of collector current available to supply this charge. With this balanced loading condition the output rise time for a step input (approximately CV/I since the output swing is limited to a small part of the collector supply voltage) is about 30 mµS. This makes possible a standard Atlas pulse duration (at 50% amplitude) of 100 mµS.

## 2.2. Classification of input gates.

Each inverter circuit is preceded by an input system. The general scheme is x identical AND-gates whose outputs are mixed together by an OR-gate. The number of AND-gates (i.e. the number of inputs to the OR-gate) is called the number of 'entries'; the number of inputs to each AND-gate is called the number of 'inputs'.
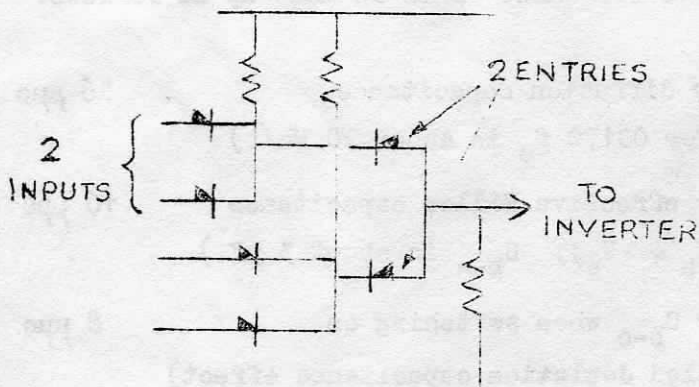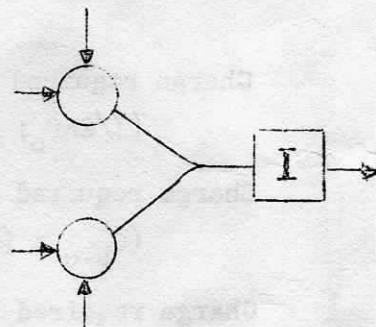


Fig. 2A          Fig. 2B.

Fig. 2a is a diagram of a typical inverter input, and Fig. 2b the logical diagram equivalent. This would be referred to as a 'two-entry two-input inverter'.

Note that in the case of single-entry circuits, where an OR-gate is

4.

not logically necessary, an OR-gate diode is always provided in order
to back off the voltage-drop in the AND-gate diodes.

Since Atlas is a parallel machine, it is often necessary to gate
the wires carrying the various digits of a number with the same waveform.
For this purpose two-input AND-gates are used, one input on each gate
being used for an information digit, the other digit on each of a number
of gates being joined together and taken to a common package pin for
connection to the controlling signal. Gates with such a connection are
known as 'strobed' gates. The controlling waveform is known as a strobe
and is supplied by a strobe emitter follower (see below).

If an internal single-input entry is provided in addition to the
other entries (of any kind) to an inverter, two such inverters may be
cross-connected via these entries to form a flip-flop. If this cross-
connection is 'wired-in' the package is known as a flip-flop package; if
it is not, the package continues to be known as an inverter package.
The additional single-input entry is ignored for 'entry, input'
classification purposes.

### 2.3 The inverter packages.

There are ten types of inverter package, differing in the input
gating and the consequent number of elements on a package. These are
tabulated below:

| | | Inputs | | | | Type | No. on Package |
|---|---|---|---|---|---|---|---|
| * | 1 | entry | 1 | input | strobed | 821 | 12 |
| * | 2 | entry | 1 | input | strobed | 831 | 8 |
| * | 3 | entry | 1 | input | strobed | 836 | 6 |
| | 1 | entry | 2 | input | | 854 | 8 |
| | 1 | entry | 5 | input | | 855 | 4 |
| | 1 | entry | 8 | input | | 856 | 3 |
| + | 12 | entry | 2 | input | | 815 | 1 |
| | 6 | entry | 2 | input | | 816 | 2 |
| | 2 | entry | 2 | input | | 817 | 5 |

*  Versions of these packages are available under different
        numbers, either cross-connected as flip-flops or without
        collector loads as cable drivers.

     +  A version of this package with fused information input
        connections is available as type 861.

### 2.4  The long-tailed pair packages.

An Atlas long-tailed pair circuit consists essentially of a
standard inverter circuit with the emitter catching diode replaced by a
second transistor.  This is shown in Fig. 3 (for a complete circuit see,
for example, Drg. 65/52824/5.).  Both transistors are OC170's.
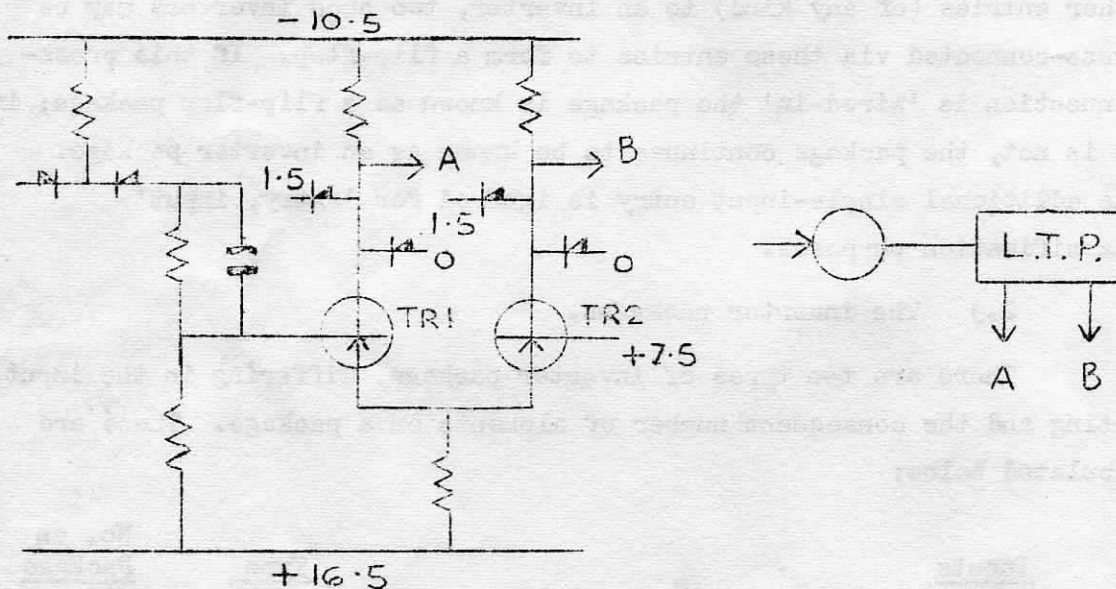


Fig. 3.

The operation of the first transistor is the same as for the
standard inverter circuit.  For a positive input, TR1 is cut off since its
base potential is about 1/2 volt more positive than the base of TR2; 8mA
then flows through TR2.  The collector of TR1 is caught at about -1/2 volt.
For a negative input, the TR1 base becomes more negative than the base of
TR2, and the current of 8mA. is then switched through TR1;  the collector

6.

moves positively and is caught at about +2v. The signal at point
A is thus the inverse of the input signal.

The collector load of TR2 is exactly the same as the inverter
circuit, with the same catching voltage. The signal at point B is thus
the same as the input signal.

There are three long-tailed pair packages, distinguished by their
input gating:

| Input | | | | Type | No. on Packages |
|---|---|---|---|---|---|
| 1 | entry | 2 | input | 825 | 6 |
| 2 | entry | 2 | input | 834 | 4 |
| 3 | entry | 2 | input | 839 | 3 |

In addition, there is a version of the 825 packages which uses TR1
as a cable driver. This is known as type 824.

Loading and rise-time considerations for each output of the long-
tailed pair are the same as for the standard inverter.

2.5    The flip-flop packages.

2.5.1 Normal flip-flops.

The strobed inverter packages 821, 831 and 836 have counterparts
provided with an additional internal single-input entry on each inverter,
pairs of inverters being internally cross-connected to make flip-flops.
The packages are:

| Inputs to each side | | | | Type | Flip-flops per package |
|---|---|---|---|---|---|
| 1 | entry | 1 | input strobed | 822 | 6 |
| 2 | entry | 1 | input strobed | 832 | 4 |
| 3 | entry | 1 | input strobed | 837 | 3 |
| 2 | entry | 1 | input strobed ⎫ | 838 | 3 |
| 1 | entry | 1 | input unstrobed ⎭ | | |

Identical strobing points on all elements on a package are brought
out to a common pin connection.

### 2.5.2  Accumulator flip-flop

For the construction of the registers of the accumulator, which need complex gating and strobing facilities, package type 819 has been designed.  Again the basic circuit consists of two standard OC170 inverters.  The logical circuit is shown in Fig. 4.  This package has the maximum amount of useful gating consistent with mounting two flip-flops on one 32-pin package.  The strobe connections are common to both elements on the package.
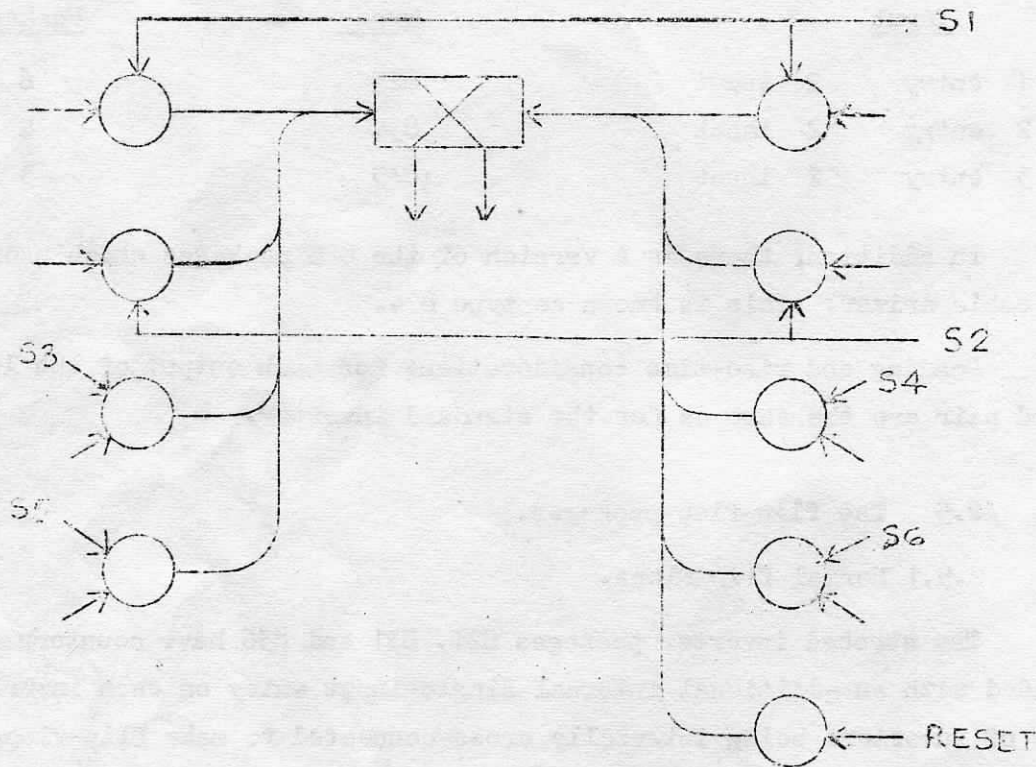


Fig 4.

### 2.6  Cable drivers and receivers.

### 2.6.1 General.

Pulse connections between packages in different boxes and different racks are made via 50Ω co-axial cable.  Packages are available for driving such lengths of cable and for terminating them correctly at the receiving end.

8.

The basic circuit of a driver with cable and receiver is shown in Fig. 5. The driver circuit consists essentially of a standard OC170 inverter with its collector resistor and catching diode replaced by the co-axial cable, which presents a collector impedance of about 50Ω. The receiver consists of an earthed-base amplifier. The effective input impedance presented to the cable is about 47Ω, representing a satisfactory match.



DRIVER
(E.G. 820)

50 Ω COAX CABLE

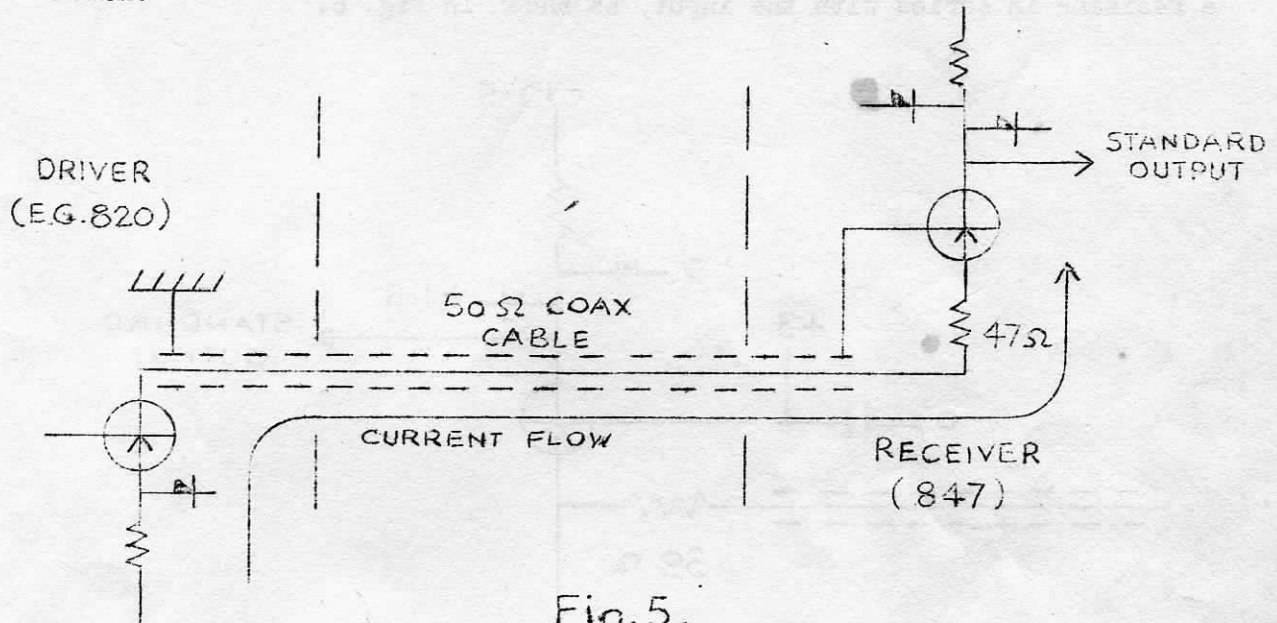CURRENT FLOW

STANDARD OUTPUT

47Ω

RECEIVER
(847)

Fig. 5.

2.6.2   The cable driver packages.

The strobed inverter packages 821, 831 and 836 have counterparts which lack the normal collector resistor and catching diodes. These cable driver packages are:

| Inputs. | | | | Type | No. on Package |
|---------|---|---|---|------|---------|
| 1 entry | 1 input | strobed | | 820 | 12 |
| 2 entry | 1 input | strobed | | 830 | 8 |
| 3 entry | 1 input | strobed | | 835 | 6 |
| 1 entry | 2 input | unstrobed | | 853 | 8 |

In addition long-tailed pair package 825 (1 entry 2 input) is available with its inverted output arranged for cable driving. This package is known as type 824.

2.6.3   The cable receiver package (Type 849)

This package contains 13 identical circuits, converting a co-axial input into a standard output. Note that the output signal from the cable receiver is in opposite phase to the input signal at the cable driver.

The effective input impedance of the earthed-base transistor is almost negligible. This is padded out to the cable impedance by means of a resistor in series with the input, as shown in Fig. 6.
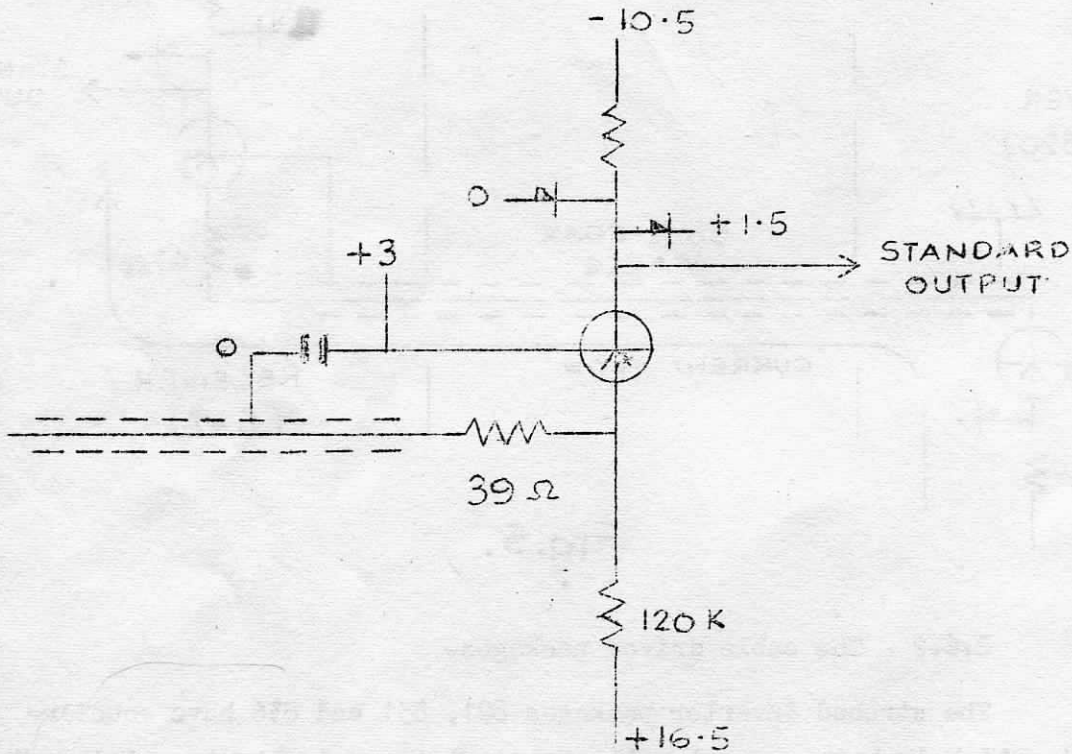


Fig. 6.

3.      THE STROBE DRIVER AND STROBE EMITTER FOLLOWER PACKAGES.

3.1   The strobe system.

As has been mentioned in 2.2, since Atlas is a parallel machine it is often necessary to open a large number of gates with the same control pulse. Since the output of the normal logical element, the inverter, will only open one gate, such an output must be amplified in order to use it for such a 'strobing' purpose.

10.

The inverter producing the control pulse feeds a power amplifier, known as a 'strobe driver'. The current output of this is sufficient to drive up to eight 'strobe emitter followers', and the output of one such strobe emitter follower will open up to eight AND-gates (normally on one package, with the common strobe connection brought out to one pin). This is shown in Fig. 7.
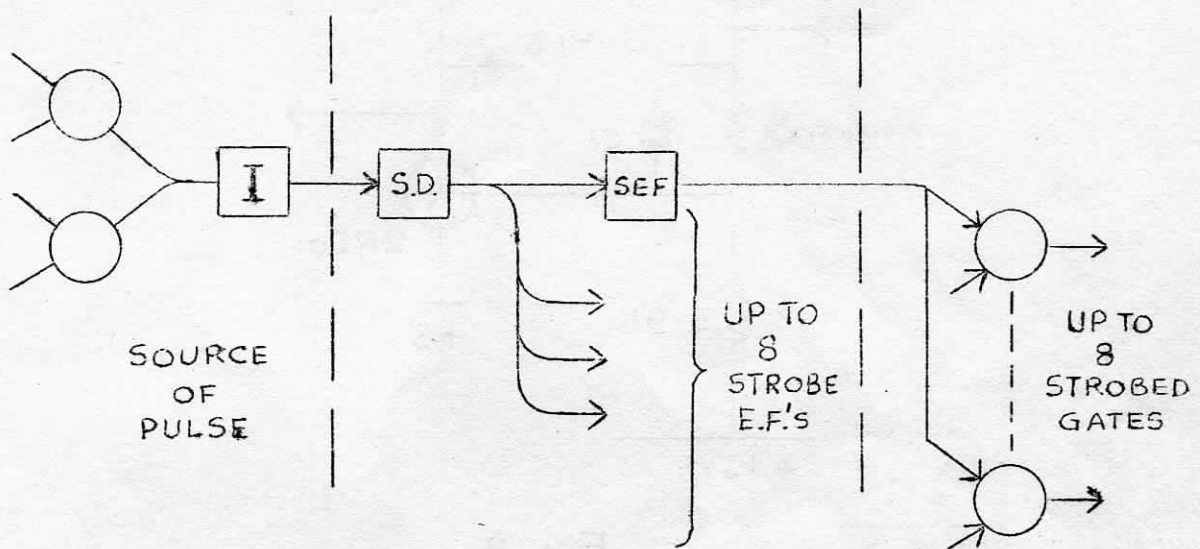


SOURCE OF PULSE

UP TO 8 STROBE E.F.'s

UP TO 8 STROBED GATES

Fig.7.

### 3.2 The strobe driver package (Type 847)

This package contains 8 identical circuits, the circuit being shown in Fig. 8.

The transistor used is a 2N501 MADT transistor; unlike the OC170, this transistor may be bottomed and still provide a sufficiently fast turn-off time.

Because of the low $\beta$ of this transistor, a relatively high base current is necessary. The input network provides a low impedance potentiometer to change the DC level of the input signal, while only requiring a low current (2mA for a +2 volt input, 1/2 mA for −1/2 volt input) from

the signal source, the majority of the potentiometer current being
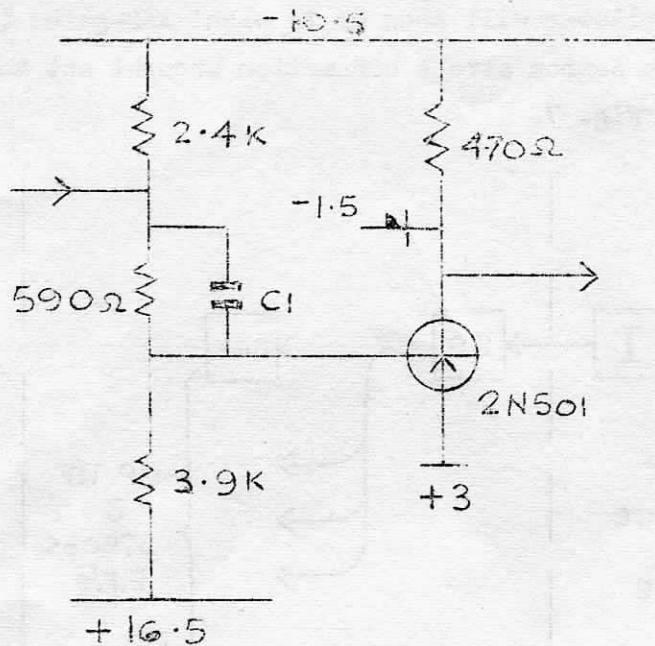derived from the power supply lines.



Fig. 8.

For +2 volt input, the transistor base is at about +3.9 volts;
since the emitter is held at +3 volts this provides an adequate cut-off
safety margin. The transistor is cut-off and the output is caught at
about - 2 volts; the current in the collector resistor is about 18mA.

For -1/2 volt input, the base potential becomes about 300 mV
negative with respect to the emitter, and the transistor conducts.
Sufficient base current flows to bottom the transistor, whose collector
moves to about + 2.5 volts. The collector current is about 28 mA.

For a positive-going input pulse of about 2.1/2 volts amplitude,
a negative pulse of about 4.1/2 volts amplitude is produced.

Although the collector current is nearly four times as great as
for the OC170 inverter, switching charge considerations are very
similar, because the diffusion capacitance term ($1/2\pi f_0$) is still only

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about 14μμc.   The switching charge is supplied by C1, a 56 pf capacitor.

The normal loading for a strobe driver element is eight strobe
emitter followers.

3.3.    The strobe emitter-follower package (Type 846)

This package contains 12 identical circuits, the circuit being
shown in Fig. 9.
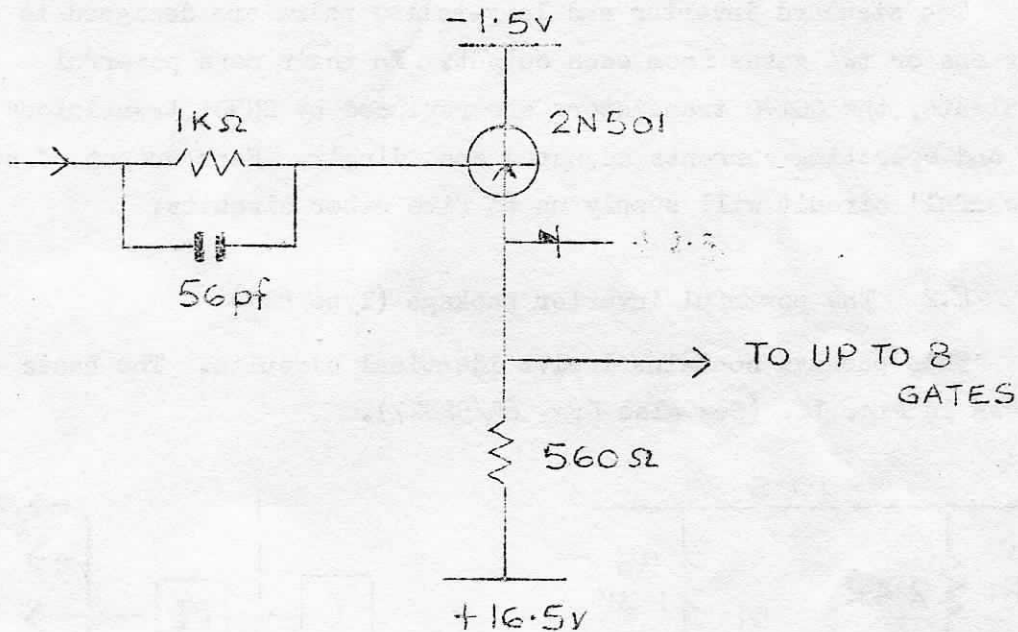


For a +2.5v input, the transistor is cut-off since its emitter is
caught positively at about +2v. About 26mA flows in the emitter resistor.

For a -2v input, the transistor bottoms and the output moves to
about -1 volt.   The input current is about 1mA for a typical transistor.
About 32mA flows in the emitter resistor; about 16mA of this is provided
by the diode gates when these are conducting.   A balanced load condition

13.

thus exists.

This circuit is not a true emitter-follower, since the transistor is bottomed and cut-off at the extremes of the input pulse. It does however provide an output of the same polarity as the input.

# 4. POWERFUL INVERTERS AND POWERFUL LONG-TAILED PAIRS.

## 4.1 General.

The standard inverter and long-tailed pairs are designed to supply either one or two gates from each output. In their more powerful equivalents, the OC170 transistors are replaced by 2N501 transistors and loads and operating currents adjusted accordingly. Each output of such a 'powerful' circuit will supply up to five other circuits.

## 4.2 The powerful inverter package (Type 827)

This package contains twelve identical circuits. The basic circuit is shown in Fig. 10. (See also Drg. 65/52827).
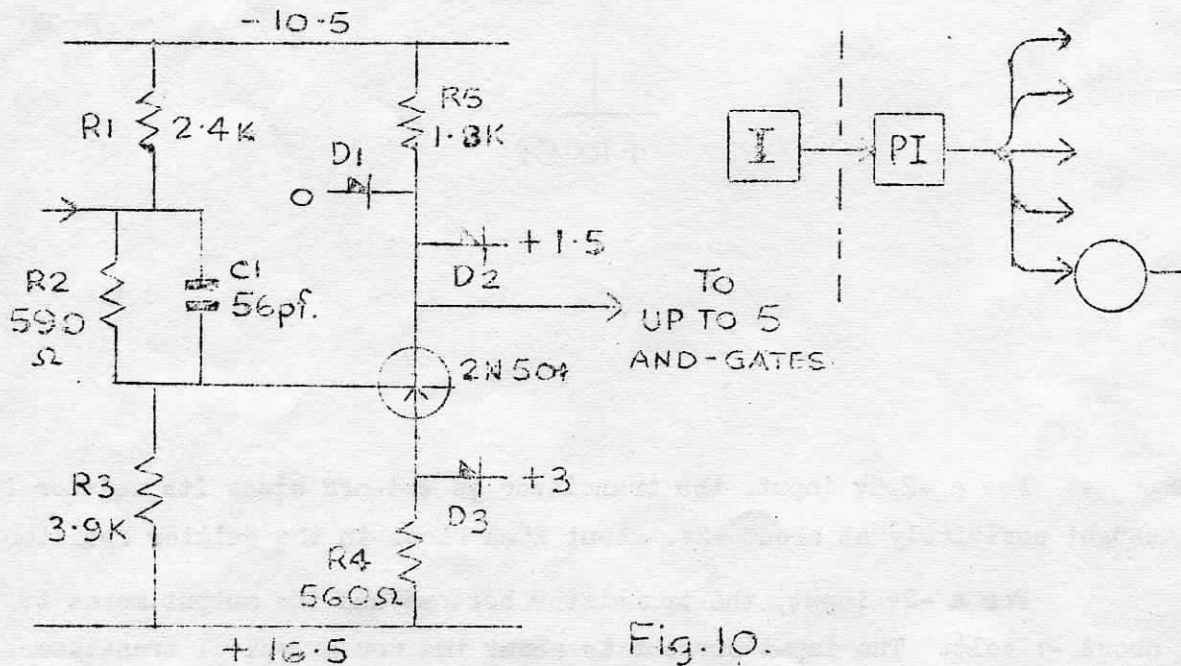


Fig. 10.

The input pin is normally connected to the standard output levels of an inverter or a long-tailed pair, i.e. -1/2 or + 2 volts. The emitter

14.

of the 2N501 transistor is caught at about +3.5 volts by D3 and the +3v. supply, and the value of the emitter resistor is such that a current of about 23mA is defined in it.

The values of R2 and R3 are arranged to provide a base potential about 0.5 volts positive with respect to the emitter when the transistor is cut-off by a standard positive input. The resistor R1 provides most of the current in the potentiometer R2/R3 so that the current drawn from the signal source is only about 2mA, despite the comparatively low resistance potentiometer. In this cut-off condition the output voltage is tied to about -1/2 v. by D4.

With a negative input level, the base voltage moves negative with respect to the potential at which the emitter is caught, and the transistor conducts. The 23 mA previously defined in the emitter resistor is switched through the transistor, whose collector potential moves positively until it is caught at about +2v by D5. The base potential now depends on the values of the input potentiometer and on the $I_b$ required to provide about 26mA. collector current. With an average value of $\beta$, the change in base potential for the two standard input levels is about 2.2 volts. The input current for a negative input is about 0.5 mA.

As in the case of the standard inverter, C1, a 56pf capacitor, supplies the charge needed to switch the transistor.

The current in the collector load, R5, is about 14mA when the transistor is conducting. The remaining collector current (12mA) supplies the gates to which the powerful inverter is connected, and charges the stray capacitance.

A powerful inverter output will supply up to five other logical elements. One inverter or long-tailed pair output is normally used to feed only one powerful inverter.

4.3    The powerful long-tailed pair package   (Type 826).

This package contains six identical circuits. The basic circuit is shown in Fig. 11. (See also Drg. No. 65/52826).
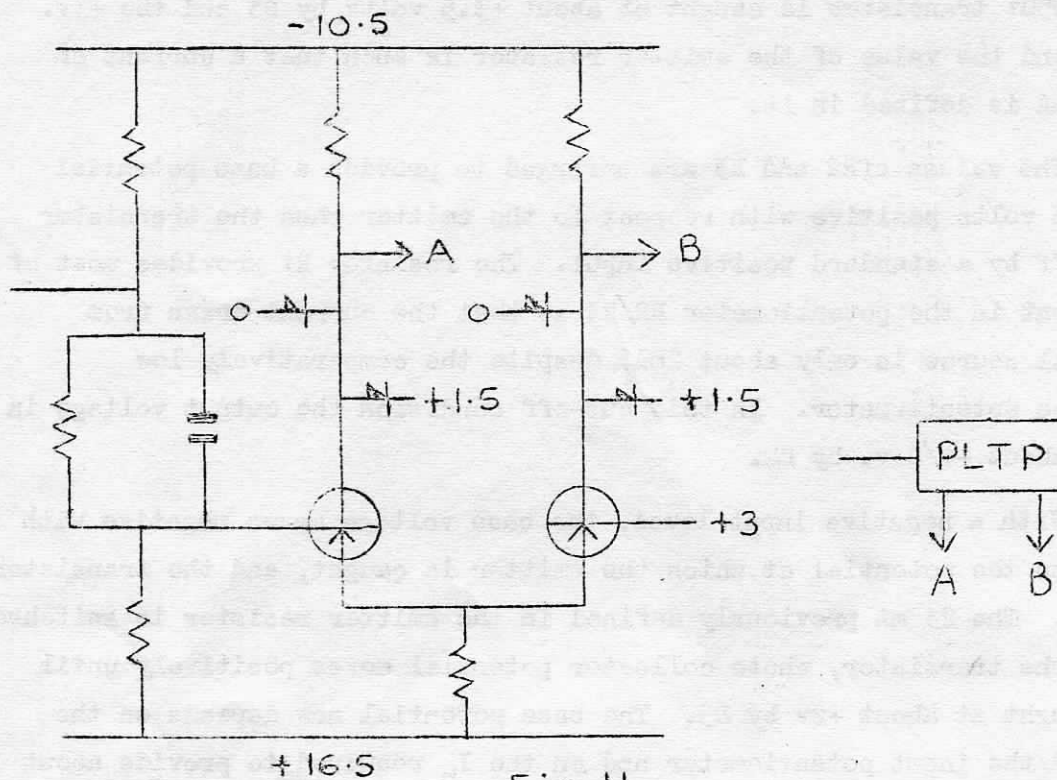
Fig.11.

The circuit consists essentially of a powerful inverter circuit
with the emitter catching diode replaced by a seond transistor. Point
A provides a signal of opposite polarity, and point B a signal of the
same polarity, as the input signal, with standard output levels.

Loading considerations are the same as for the powerful inverter.

5.        DECODER EMITTER-FOLLOWERS.

The basic decoder circuit consists of a 2, 5 or 8 - input AND-gate
followed by an emitter follower, as shown in Fig. 12 (a complete circuit
may be found on, for example, Drg. 65/52851).

Because of the low base current requirement of the emitter follower,
the load resistor of the AND-gate is higher than in the normal AND-gate.
The load current is thus only 0.4 mA and several decoder gates may be fed
from a single inverter or long-tailed pair output.

Since no backing-off diode is used, the signal levels at the base of
the transistor are about 1/2 volt more negative than the gate input levels;
16.

but because the base-emitter volt drop in the emitter follower is of the same order, the output levels are substantially standard.
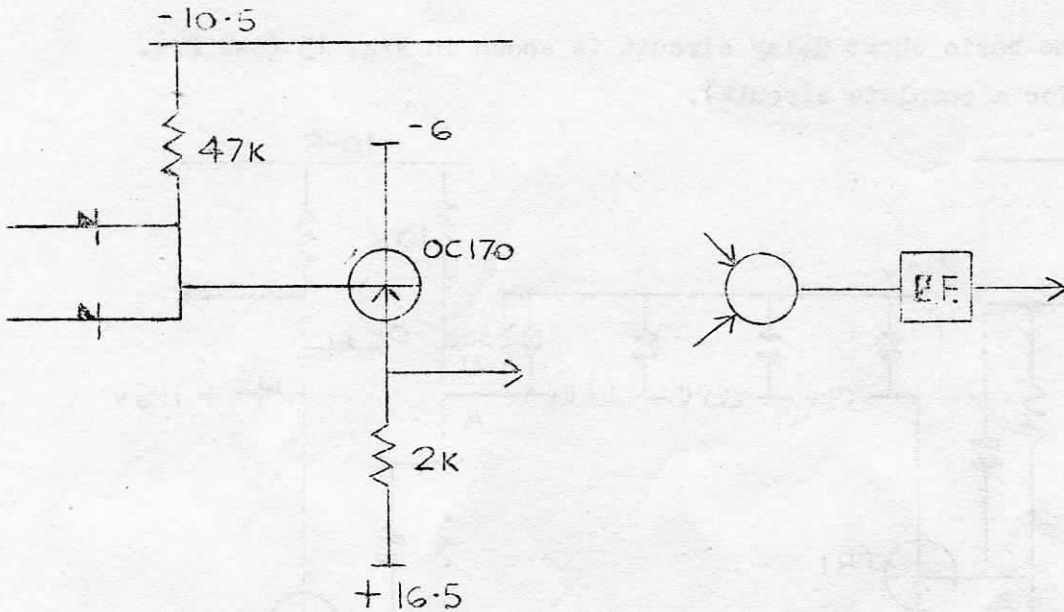


Fig. 12.

The transistor operates in true emitter-follower mode, and provides fast rise and fall times with normal stray capacitance loading. The emitter current is about 8mA, and the collector voltage is -6 volts to limit the transistor power dissipation.

There are three decoder packages, with different input gate provisions:

| No. of inputs | | Type | No. on packages |
|---|---|---|---|
| 2-input | AND-gate | 850 | 8 |
| 5-input | AND-gate | 851 | 4 |
| 8-input | AND-gate | 852 | 3 |

# 6.    THE DELAY PACKAGES.

### 6.1    The short delay circuit.

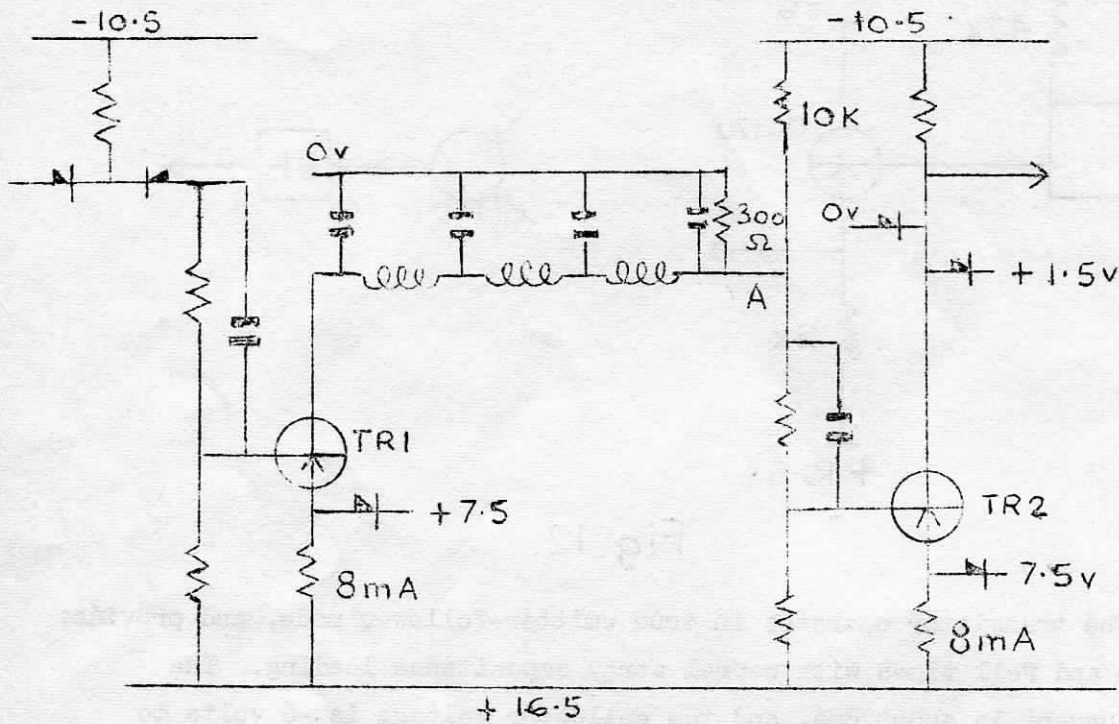The basic short delay circuit is shown in Fig. 13 (see Drg. 65/52843 for a complete circuit).



Fig. 13.

The input circuit consists of convential AND-gate and OR-gate diodes so that signals to the input potentiometer are at standard levels. TR1 is a standard OC170 inverter with its collector circuit replaced by a three-section lumped-constant delay line, terminated by a 300Ω resistor.  TR2 is a fully standard OC170 inverter.

With +2v. at the input potentiometer of TR1, TR1 is cut-off, amd a current of 8mA flows in its emitter resistor via the catching diode and the +7.5v. supply.  The potential at point A is then about -0.3 volts. This allows TR2 to conduct and its output potential is caught at +2v.

18.

If a negative stop is then applied, TR1 conducts and this current flows into the delay line. After a delay determined by the constants of the delay line, this current flows in the 300Ω resistor and point A moves to about +2v. This cuts off TR2 and causes its output to be caught at -1/2v.

A subsequent positive step cuts off TR1 and after a similar delay TR2 starts to conduct. An input pulse is therefore reproduced at the output of the circuits after a delay.

The magnitude of the delay depends on the characteristics of the delay line. Separate plug-in assemblies are available for 60, 80, 100 and 120 millimicroseconds.

### 6.2  The long delay circuit.

The basic long delay circuit is shown in Fig. 14 (for a complete circuit see Drg. 65/52804).
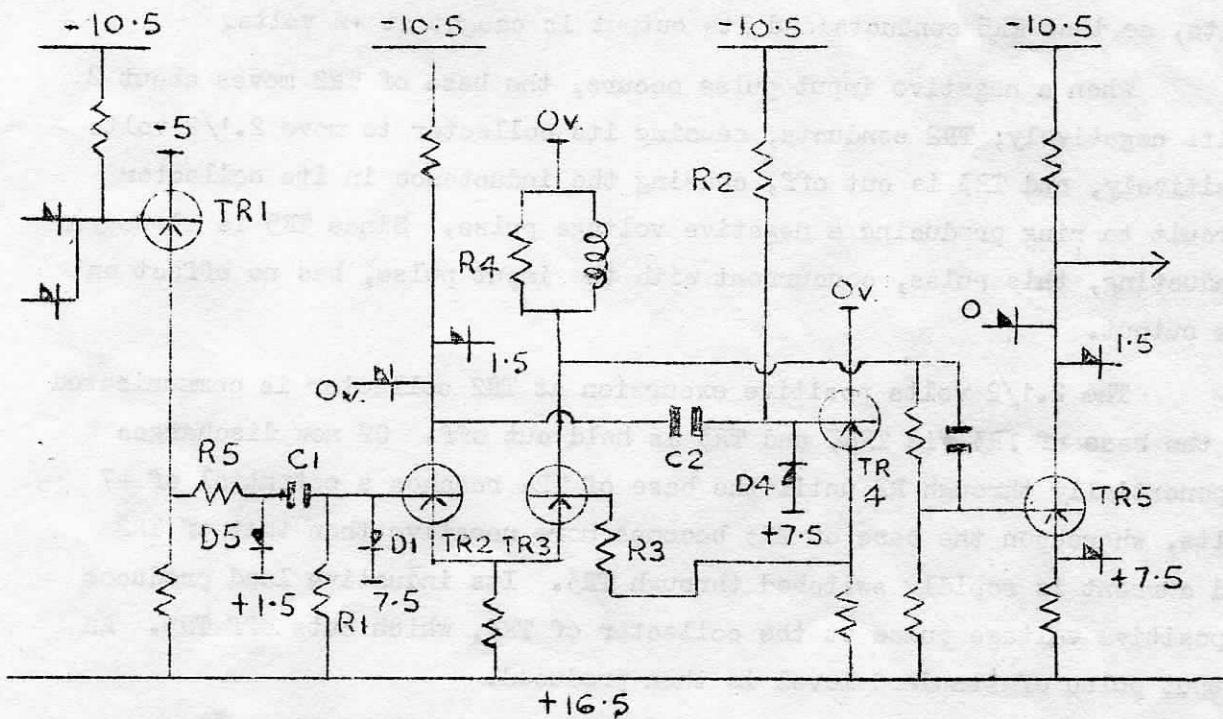


Fig. 14.

The input stage consists of an AND-gate followed by an emitter follower, TR1. For a standard negative input pulse, a pulse of almost the same amplitude is produced at the emitter of TR1.

R5, D5 and the +1.5 volt supply form a limiter circuit which removes any small negative-going castellations (which may be caused by imperfect gating) from the output of the emitter follower. The pulse amplitude is thus reduced to about 2 volts (-1/2v. to +1.5v.).

C1, R1 and D1 form together with the +7.5v. supply a D.C.restorer tying signals to the base of TR2 positively at about +8v.

TR2 and TR3 form an emitter-coupled (long-tailed pair)monostable circuit, the timing circuit being C2 R2. Emitter-follower TR4 is used as a buffer between the timing circuit and the relatively low input impedance of TR3, to increase the maximum permitted value of R2 (to 18KΩ). In the stable state D4 ties the emitter of TR4 to about +7.5 volts; since this is more negative than the base voltage of TR2, TR3 conducts and TR2 is cut off. The input to the potentiometer of inverter TR5 is about 0 volts, so that TR5 conducts and its output is caught at +2 volts.

When a negative input pulse occurs, the base of TR2 moves about 2 volts negatively; TR2 conducts, causing its collector to move 2.1/2 volts positively, and TR3 is cut off, causing the inductance in its collector circuit to ring producing a negative voltage pulse. Since TR5 is already conducting, this pulse, concurrent with the input pulse, has no effect on the output.

The 2.1/2 volts positive excursion at TR2 collector is communicated to the base of TR3 via TR4, and TR3 is held cut off. C2 now discharges exponentially through R2 until the base of TR4 reaches a potential of +7 volts, whereupon the base of TR3 becomes more negative than that of TR2 and current is rapidly switched through TR3. Its inductive load produces a positive voltage pulse at the collector of TR3, which cuts off TR5. An output pulse of standard level is then produced.

The inductance in the collector circuit of TR3 is critically damped by R4 (820 Ω) to produce a single output pulse. The width of the pulse is adjusted to a nominal 100 mμ.sec. by means of a ferrite slug.

20.

The delay between input and output pulse depends on the value of C2, whose maximum value is limited in turn by considerations of physical size and the spacing between packages. The normal value of delay used in Atlas is 300 mµSec., this being the maximum time for an adder operation.

6.3   The delay package types.

There are at present four package types using delay circuits. These are:-

(a)   Type 843:  Delay Package Type 6.

This package contains three short delay circuits, two being 2-input 2-entry and one 1-input 5-entry (Fig. 15).



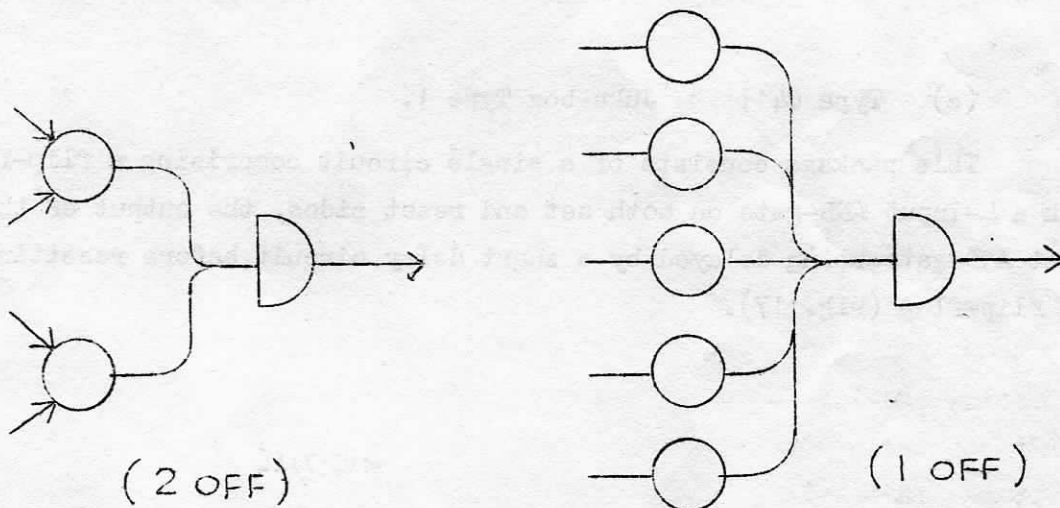( 2 OFF )                    ( I OFF )

Fig. 15.

(b)   Type 804:  Fixed store rhythm unit delay package.

This package contains two identical short delay circuits (single entry two input) and one long delay circuit (single entry single input) together with a modified powerful inverter (Fig. 16).
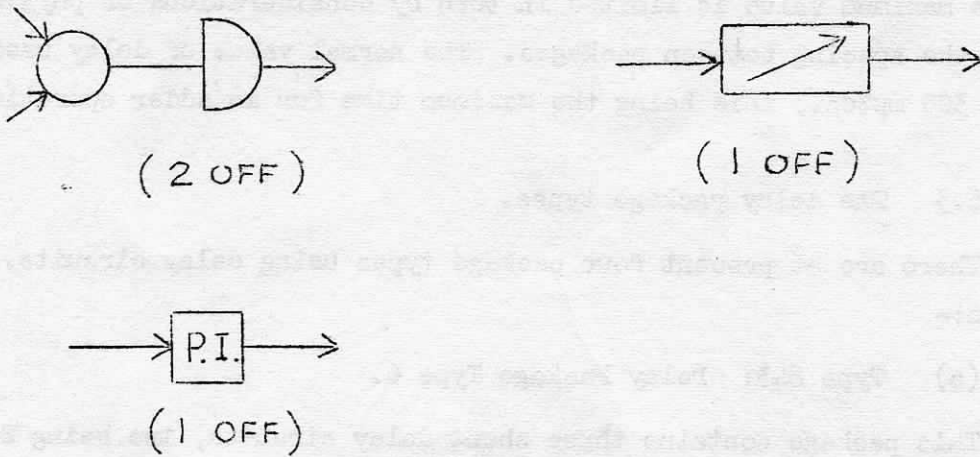
( 2 OFF )

( 1 OFF )

P.I.

( 1 OFF )

Fig. 16.

(c)  Type 841:  Juke-box Type 1.

This package consists of a single circuit comprising a flip-flop
with a 4-input AND-gate on both set and reset sides, the output of the
reset AND-gate being delayed by a short delay circuit before resetting
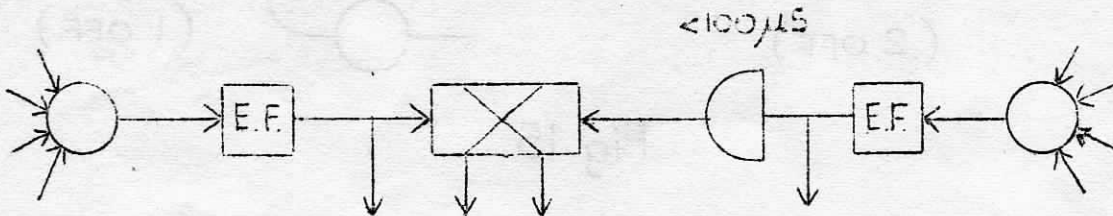the flip-flop (Fig. 17).

<100μS

E.F.       ✕       E.F.

Fig. 17

This circuit is commonly used in the manner shown in Fig. 18 to
produce a single output pulse when two operations are complete.

22.

INPUT A

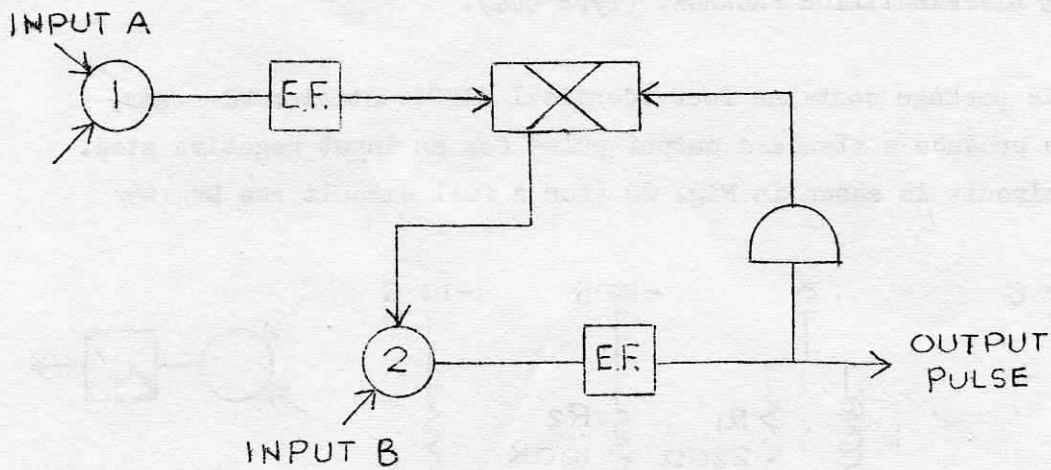E.F.

OUTPUT PULSE

INPUT B

Fig. 18.

Input A sets the flip-flop and primes gate 2. When input B occurs the gate opens and an output is produced. After a time determined by the delay used and the switching time of the flip-flop (normally about 100 muSec. altogether) the flip-flop is reset, closing the gate and terminating the output. A short duration output pulse is thus produced.

(d)    Type 842:    Delay board Type 1.

This package consists of two identical long-delay circuits, each single-entry two-input. An external output is available immediately after the emitter follower (i.e. before the clipper circuit shown in Fig. 14 as R5, D5). This is shown in Fig. 19.
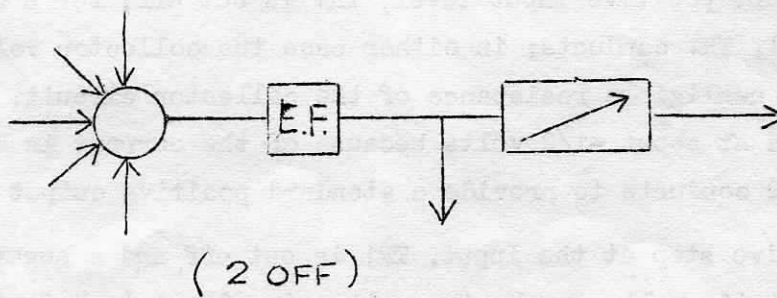


E.F.

( 2 OFF )

Fig. 19.

7.    THE DIFFERENTIATOR PACKAGE. (Type 844).

This package contains four identical differentiator elements,
designed to produce a standard output pulse for an input negative step.
The basic circuit is shown in Fig. 20 (for a full circuit see Drg.65/
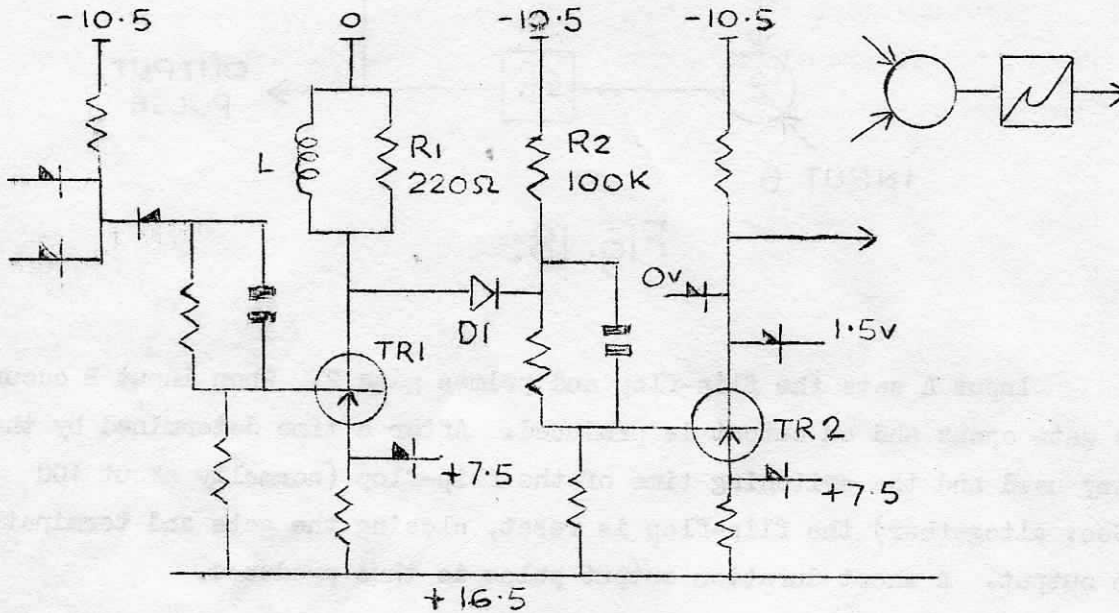52844).



Fig. 20

The input circuit consists of a standard inverter with its
collector load replaced by a critically damped inducter/resistor
combination (L,R1).

For a constant positive input level, TR1 is cut off; for a constant
negative input level, TR1 conducts; in either case the collector voltage
is 0 because of the negligible resistance of the collector circuit.  The
junction of D1/R2 is at about -1/2 volts because of the current in D1 and
R2, and inverter TR2 conducts to provide a standard positive output level.

For a positive step at the input, TR1 is cut off and a negative
pulse is produced at its collector by the collapsing field in L (critically
damped by R1 so that only one pulse is produced).  Since however TR2 is
already conducting, this pulse has no effect on the output level.

24.

For a negative step at the input, TR1 conducts and a positive pulse is produced at its collector. For the duration of this pulse TR2 is cut off and a negative pulse of standard level is produced at the output.

For a negative input step, there is thus produced a negative output pulse. The duration of this pulse is varied by adjustment of a ferrite slug in L.